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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,913	03/30/2004	Paul Hanrieder	57983.000165	3176
21967 75	590 07/14/2006	EXAMINER		
	WILLIAMS LLP	BAE, JI H		
INTELLECTU 1900 K STREE	AL PROPERTY DEPART ET, N.W.	ART UNIT	PAPER NUMBER	
SUITE 1200		2115		
WASHINGTO	N, DC 20006-1109	DATE MAILED: 07/14/2006		

Please find below and/or attached an Office communication concerning this application or proceeding.

			Application No.		Applicant(s)			
Office Action Summary			10/811,913		HANRIEDER ET AL.			
		<u> </u>	Examiner		Art Unit			
			Ji H. Bae		2115			
Period fo	 The MAILING DATE of this community Reply 	cation appea	ars on the cover shee	et with the co	orrespondence ad	ddress		
WHIC - Exter after - If NC - Failu Any	ORTENED STATUTORY PERIOD FO CHEVER IS LONGER, FROM THE MA nations of time may be available under the provisions o SIX (6) MONTHS from the mailing date of this commu period for reply is specified above, the maximum state re to reply within the set or extended period for reply we reply received by the Office later than three months afted patent term adjustment. See 37 CFR 1.704(b).	AILING DAT of 37 CFR 1.136 (inication. utory period will vill, by statute, ca	E OF THIS COMMU (a). In no event, however, ma apply and will expire SIX (6) ause the application to become	UNICATION ay a reply be time MONTHS from the ne ABANDONED	.' ely filed the mailing date of this	,		
Status								
1)[🛛	Responsive to communication(s) filed	l on <i>30 Mar</i>	rch 2004.					
· —	This action is FINAL . 2b)⊠ This action is non-final.							
3)	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is							
,_	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.							
Dispositi	on of Claims					·		
4)⊠	Claim(s) <u>1-20</u> is/are pending in the application.							
	4a) Of the above claim(s) is/are withdrawn from consideration.							
	Claim(s) is/are allowed.							
·	Claim(s) 1-20 is/are rejected.							
	Claim(s) <u></u>							
·	Claim(s) are subject to restriction and/or election requirement.							
Applicati	on Papers							
	•	Evaminar						
9) The specification is objected to by the Examiner.								
10) The drawing(s) filed on 30 March 2004 is/are: a) accepted or b) objected to by the Examiner.								
	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.								
	ınder 35 U.S.C. § 119	by the Exam	Timor. Note the attac	oned Omee /	Action of form 1	10-102.		
	•			0 0 4 4 0 4 3	(1)			
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 								
2) Notice (3) Information	t(s) e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PT mation Disclosure Statement(s) (PTO-1449 or P r No(s)/Mail Date		Paper 5)	iew Summary (· No(s)/Mail Dat e of Informal Pa :		O-152)		

DETAILED ACTION

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 14-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 14 recites a method for storing data. However, the steps recited by the claim do not actually accomplish the storing of data. The claimed method merely "permits" stored data to be transferred from the high speed volatile memory to the non-volatile memory when power is above a minimum voltage level, and "prevents" the same when power is below a minimum voltage level. The method itself does not actually perform any storing or transferring steps per se; it merely permits or prevents them. As a result, the claimed method lacks a useful, concrete, and tangible result, and is therefore deemed non-statutory.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1-20, applicant has variously recited a "high speed non-volatile electronic memory configuration", or a "high speed volatile memory". Applicant's usage of the term "high speed" in the claim language renders the scope of the claims indefinite, as the term

itself is highly subjective. Applicant's specification provides no measurable, quantifiable, or otherwise specific criteria for determining what constitutes a "high speed" memory. In particular, the examiner points out that it is the nature of the art that what was once considered "high speed" is quickly rendered slow and obsolete within a few years.

Regarding claim 14, the claim recites a method for storing data that "permits" data to be transferred from a high speed volatile memory to a non-volatile memory when power is above a minimum voltage level. Applicant's use of the word "permit" renders the scope of the claim so broad that it renders the claim indefinite. In particular, the examiner points out that anything that does not expressly prohibit the transfer of data from a volatile memory to a non-volatile memory while power is above a minimum operating voltage may be said to "permit" such a transfer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Strasser, U.S. Patent No. 6,990,603, in view of Taylor et al., U.S. Patent No. 6,263,398 B1.

Regarding claim 1, Strasser teaches:

- a high speed volatile memory [Fig. 1, volatile memory 220];
- a non-volatile memory coupled to the high speed volatile memory [non-volatile memory 230];

a controller coupled to the high speed volatile memory and the non-volatile memory that controls transfer of data from the high speed volatile memory to the non-volatile memory when

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power is above a particular minimum operating voltage level [control unit 210, also Fig. 4, col. 7, lines 26-37]; and

a power level detector that detects when power is above the minimum operating voltage level [col. 7, lines 39-41].

Strasser does not teach that the controller monitors data storage changes made in the high speed volatile memory.

Taylor teaches a memory system employing a non-volatile memory coupled to a cache [Fig. 1], employing a "write-through" caching technique. The system monitors writes to the cache and reflects the changes made to the cached data in the non-volatile memory [col. 8, lines 16-18, 59 to col. 9, line 16].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Strasser and Taylor by modifying the controller of Strasser to monitor for data changes in the volatile memory, as taught by Taylor. Both Strasser and Taylor teach memory systems comprised of a volatile memory and a slower, non-volatile memory that holds a copy of the data in the volatile memory. Strasser teaches that the backing up of the volatile memory occurs periodically while the minimum power is maintained, but does not how often. The teachings of Taylor would improve the system of Strasser by triggering writes to the non-volatile memory upon detecting changes to the volatile memory (e.g. write through), thus ensuring that the non-volatile memory accurately reflects the latest changes made to the volatile memory.

Regarding claim 2, Strasser teaches a power storage element that stores transient power for use by at least one of the high speed volatile memory, the non-volatile memory, and the controller when power is below the particular minimum operating voltage level [uninterruptible power supply 240, Fig. 2].

Regarding claim 3, Strasser teaches that the power from the power storage element is used to transfer the stored data in the volatile memory to the non-volatile memory when power is below the particular minimum operating level [col. 5, lines 48-50].

Regarding claim 4, it would have been obvious to use a capacitor with capacitance in the hundred of microfarads as a matter of design choice.

Regarding claim 5, it would have been obvious to use a dynamic RAM for the high speed volatile memory. DRAM is a well-known and commonly used volatile memory.

Regarding claim 8, Taylor teaches that the non-volatile memory is a low speed non-volatile memory relative to the high speed volatile memory [col. 2, lines 30-33].

Regarding claim 9, Strasser teaches that the non-volatile memory is a non-volatile flash memory [claim 19].

Regarding claim 10, Strasser teaches that the controller is one of a microprocessor, a microcontroller, a programmable processing device, and a fixed function processing device [claim 17].

Regarding claim 11, Strasser teaches that the controller prevents the transfer of stored data from the high speed volatile memory to the non-volatile memory, and vice versa, when power is below the particular minimum operating voltage level [UPS shut down, col. 8, lines 1-5].

Regarding claim 12, Strasser teaches that the controller controls the transfer of stored data from the non-volatile memory to the high-speed volatile memory immediately following a restoration of power to above the particular minimum operating voltage level [col. 9, lines 10-23].

Regarding claim 13, Strasser teaches that the power level detector provides an indication to the controller that power is above the particular minimum operating voltage level.

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Regarding claim 14, Strasser/Taylor teaches a method comprising:

monitoring data storage changes made within a high speed volatile memory [col. 8, lines 16-18, 59 to col. 9, line 16];

permitting stored data to be transferred from the high speed volatile memory to a non-volatile memory, and vice versa, based upon the monitored data storage changes when power is above a particular minimum operating voltage level [col. 7, lines 26-37]; and

preventing stored data to be transferred from the high speed volatile memory to the non-volatile memory, and vice versa, when power is below the particular minimum operating voltage level [UPS shut down, col. 8, lines 1-5].

Regarding claim 15, Strasser teaches detecting when power is above the particular minimum operating voltage level.

Regarding claim 16, Strasser teaches providing an indication that power is above the particular minimum operating voltage level.

Regarding claim 17, Strasser teaches detecting when power is below the particular minimum operating voltage level.

Regarding claim 18, Strasser teaches providing an indication that power is below the particular minimum operating voltage level.

Regarding claim 19, Strasser teaches providing a transient power when power is below the particular minimum operating voltage level [uninterruptible power supply 240, Fig. 2]; and

permitting stored data to be transferred from the high speed volatile memory to a non-volatile memory based upon the monitored data storage changes for a limited period of time using the transient power when power is below the particular minimum operating voltage level [col. 5, lines 48-50].

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Regarding claim 20, Strasser teaches controlling the transfer of stored data from the non-volatile memory to the high speed volatile memory immediately following a restoration of power to above the particular minimum operating voltage level [col. 9, lines 10-23].

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Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Li et al., U.S. Patent No. 6,336,174 B1;

Byrd, U.S. Patent No. 4,763,333;

Campanale, U.S. Patent Application Publication No. 2005/0268157 A1.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ji H. Bae Patent Examiner Art Unit 2115 <u>ii.bae@uspto.gov</u> 571-272-7181